CLAIMS

What is claimed is:

1. An apparatus, comprising:

a phase controller to generate interrelated control signals based upon a comparison of a recovered clock signal with a data signal; and

a phase interpolator coupled with said phase controller to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from the more than one phase are weighted in accordance with the interrelated control signals.

2. The apparatus of claim 1, further comprising a phase-frequency detector coupled with said phase controller to sample data of the data signal at a sample rate based on the recovered clock signal and to output a comparison signal based on samples of the data.

3. The apparatus of claim 2, wherein the phase-frequency detector comprises circuitry to compare at least a pre-data bit sample, a mid-data bit sample, and a post-data bit sample to determine the comparison signal.

4. The apparatus of claim 2, wherein the phase-frequency detector comprises circuitry to modify a phase update rate based upon past phase updates over a period of time in an absence of phase updates.

5. The apparatus of claim 2, further comprising phase update logic circuitry coupled with the phase-frequency detector to generate charge and discharge signals based upon the comparison signal.

6. The apparatus of claim 5, wherein the phase update logic circuitry comprises circuitry to manage the distribution of phase updates to a phase control circuit of

said phase controller, associated with a managing interrelated control signal of the interrelated control signals.

7. The apparatus of claim 1, further comprising a reference clock coupled to said phase interpolator to output more than two phases of the reference clock signal.

8. The apparatus of claim 1, wherein said phase controller comprises more than one phase control circuit to generate voltage signals as the interrelated control signals.

9. The apparatus of claim 1, wherein said phase controller comprises a first phase control circuit to generate a first interrelated control signal of the interrelated control signals and a second phase control circuit to generate a second interrelated control signal of the interrelated control signals, wherein the second interrelated control signal decreases in amplitude at substantially the same rate as the first interrelated control signal increases in amplitude.

10. The apparatus of claim 9, wherein said phase controller further comprises:

charge circuitry to transition the amplitude of the first interrelated control signal higher in response to a charge signal; and

discharge circuitry to transition the amplitude of the second interrelated control signal lower in response to a discharge signal.

11. The apparatus of claim 10, wherein said phase controller further comprises:

trip high circuitry to compare the amplitude of the first interrelated control signal to a high amplitude reference; and

trip low circuitry to compare the amplitude of the second interrelated control signal to a low amplitude reference.

12. The apparatus of claim 1, wherein said phase controller comprises hysteresis circuitry to prevent chatter in an overflow signal.

13. The apparatus of claim 1, wherein said phase controller further comprises common mode feedback circuitry coupled with more than one phase control circuit to substantially compensate for changes in a common mode amplitude of managing interrelated control signals of the interrelated control signals.

14. The apparatus of claim 1, wherein said phase interpolator comprises phase control circuitry to transition the bias current, based upon the interrelated control signals, of a differential current-steering mechanism to adjust the amplitude contributions.

15. The apparatus of claim 14, wherein said phase interpolator comprises a degenerative mesh coupled with the phase control circuitry to degenerate a transfer characteristic of the phase control circuitry.

16. The apparatus of claim 15, wherein said phase interpolator further comprises circuitry to filter an output of the differential current-steering mechanism.

17. A method, comprising:

receiving a data signal;

comparing the data signal to a recovered clock signal;

generating interrelated control signals based on said comparing; and

combining amplitude contributions from phases of a reference clock signal wherein the amplitude contributions are based on the interrelated control signals, to change a phase of the recovered clock signal with an analog transition.

18. The method of claim 17, further comprising generating a charge and discharge signal based upon said comparing.

19. The method of claim 18, wherein generating a charge and discharge signal comprises generating a charge signal to increase an amplitude of a first interrelated control signal of the interrelated control signals substantially simultaneously with generating a discharge signal to decrease an amplitude of a second interrelated control signal of the interrelated control signals.

20. The method of claim 17, further comprising determining an update pattern to provide phase updates for said generating interrelated control signals in the absence of data transitions.

21. The method of claim 17, wherein said generating interrelated control signals comprises generating a first control signal and a second control signal to adjust the amplitude contributions from a first phase and a second phase of the phases of the reference clock signal, wherein adjustments to the amplitude contributions of the first phase and the second phase are substantially inversely proportional.

22. The method of claim 17, wherein said generating interrelated control signals comprises generating a first ramping control signal and a second ramping control signal, wherein an amplitude of the first ramping control signal increases at a rate

substantially equivalent to a rate that an amplitude of the second ramping control signal decreases.

23. The method of claim 17, wherein said combining comprises:

generating differential signals with at least one of the phases of the reference clock signal, based upon the interrelated control signals; and

filtering the differential signals to change the phase of the recovered clock signal with the analog transition.

24. The method of claim 23, wherein filtering comprises integrating the differential signals.

25. A system, comprising:

a front-end receiver to amplify a data signal;

a phase-frequency detector coupled with said front-end receiver to sample data from the data signal based upon a recovered clock signal and generate a comparison signal based on the sampled data;

phase update logic circuitry coupled with said phase-frequency detector to generate a signal based upon the comparison signal, to update interrelated control signals;

a phase controller coupled with said phase update logic circuitry to generate interrelated control signals based upon the signal; and

a phase interpolator coupled with said phase controller to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from the more than one phase are weighted in accordance with the interrelated control signals.

26. The system of claim 25, wherein said phase controller comprises a first phase control circuit to generate a first interrelated control signal of the interrelated control signals and a second phase control circuit to generate a second interrelated control signal of the interrelated control signals, wherein the second interrelated control signal decreases in amplitude at substantially the same rate as the first interrelated control signal increases in amplitude.

27. The system of claim 25, wherein said phase interpolator comprises phase control circuitry to transition the bias current of a differential current-steering mechanism based upon the interrelated control signals.

28. A machine-readable medium containing instructions, which when executed by a machine, cause said machine to perform operations, comprising:

receiving a data signal;

comparing the data signal to a recovered clock signal;

generating interrelated control signals based on said comparing; and

combining amplitude contributions from phases of a reference clock signal wherein the amplitude contributions are based on the interrelated control signals, to change a phase of the recovered clock signal with an analog transition.

29. The machine-readable medium of claim 28, wherein said generating interrelated control signals comprises generating a first ramping control signal and a second ramping control signal, wherein an amplitude of the first ramping control signal increases at a rate substantially equivalent to a rate that an amplitude of the second ramping control signal decreases.

30. The machine-readable medium of claim 28, wherein said combining comprises:

generating differential signals with at least one of the phases of the reference clock signal, based upon the interrelated control signals; and

filtering the differential signals to change the phase of the recovered clock signal with the analog transition.